

LEAKAGE CURRENT REDUCTION METHOD

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PRIMARY EXAMINER

5 FIELD OF THE INVENTION

The present invention relates to electronic circuitry and, in particular, to a leakage current reduction method.

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BACKGROUND OF THE INVENTION

In a prior approach for powering down a circuit system, when the system goes into sleep / data retention mode, the main power supply VDD goes from 1.3V (in active mode) to near 0V, a retaining power supply VRET remains unchanged at, for example, 1.3V, a retain signal RET goes from 0V to VRET (1.3V) level, and some internal nodes of the system are raised to a reference voltage VBB level (for example 0.6V).

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For circuits whose data needs to be retained when the system goes into sleep / data retention mode, the typical way of turning off the P Channel (PCH) device is shown below:

25 Vdrain = VBB (0V --> 0.6V, for example)

Vgate = RET (0 \rightarrow 1.3V, for example)

Vsource = VDD (1.3V --> 0V, for example)

Vbulk = VRET (1.3V , for example)

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